GaAs RELIABILITY DATABASE

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INTRODUCTION:

GaAs based MESFETs and MMIC devices exhibit excellent electrical performance in the X, Ka, and V band regions. However, these devices must also perform reliably for the duration of a space mission.

Reliability information about GaAs devices is scattered between such media as journals, papers, and conference proceedings. Thus, information about a specific device cannot be located efficiently. However, one medium to locate information efficiently is an electronic database. A database could prove to be a valuable tool to both the user and the manufacturer. From failure trends in the database, one could analyze the database to asses device reliability for a particular application. Such a database has been developed at JPL, and the following is a description of its structure and a brief summary of its contents and capabilities.

DATABASE COMPOSITION:

The database consists of two main sections, the data references and the device reliability records. The reference section contains 8 fields: reference number, date of publication, authors, article title, publisher, volume, and page numbers. The device section consists of 53 fields (Table 1) structured into two main groups. The first group contains information about the data source, manufacturer, device type, device specifications, device structure, process technology, chip mounting technique, and packaging. The second group contains information regarding sample size, screening, and test type. The test type information can be further divided into four subgroups: storage test, DC life test, RF life test, and radiation test. Each subgroup contains information about the failure criteria, test time and results, test temperature, associated activation energy, failure mode, failure mechanism, and failure analysis method.

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When working with the database, three tasks are generally considered: appending data, editing data, and searching for data . To make the database more user friendly, a user interface was added to make these tasks more efficient.

DATA **ANALYSIS:**

Reliability data from 50 references [1..50] was compiled into the database forming 100 records. A preliminary analysis of the data was conducted. The information presented below reflects the current content of the database.

Gate Metallization and Structure:

Gate metallization is a major reliability concern for GaAs devices. There are two common gate metallization materials, Al-based and Au-based.

Al-Based Schottky Gates:

Surface Effects:

Temperature cycling tests of unpassivated Al gate devices indicate a rapid decrease in I_{dss} and g_m. This is explained by the thinning of the active channel due to electrolytic corrosion [14]. However, passivating the device surface with SiO_2 has been reported to cause a rapid increase of the gate leakage current. 'l'his increase in leakage current was attributed to the metallic migration via electrolytic paths which form a metallic bridge between the source and gate.

In a comparative study, both unpassivated power MESFETs and MESFETs with a CVD SiO_2 passivation layer were subjected to gate reverse 'bias tests. Both types of MESFETs suffered from output power reduction. The failure mechanism for the unpassivated devices was identified as release of free arsenic while the failure mechanism for the SiO_2 passivated devices was described as strong oxidation which erodes the channel surface . In the same study, MESFETs with PECVD Si_3N_4 protection layer showed no output power decrease due to gate reverse bias stress [12]. However, these findings were contradicted in another reliability study which uses both gate reverse bias and RF life test. The results of this new study indicated that MESFETs with SiO_2 passivation are very stable when compared with Si_3N_4 passivated MESFETs [40].

Au/Al Intermetallic Interaction:

Direct coupling between Al and Au metallizations can result in an increase in gate resistance due to a metallurgical reaction (purple plague). An RF life test on devices with Ti metal sandwiched between the Al and Au metallizations also showed a substantial increase in the gate resistance. This increase was attributed to the formation of an oxide or hydroxide of Ti [1] .

Refractory Barrier Layer:

The reliability of Al gate devices can be improved by the inclusion of a refractory barrier between the Al gate metallization and the semiconductor. Storage tests on devices with Al/Ni gates showed an increase in barrier height due to the migration of Ni into the Al film. On the other hand, high temperature storage tests on devices with a Ti refractory barrier showed a decrease in barrier height due to the formation of Al_3Ti [10].

Au-Based Schottky Gates:

Au/Pt,W, or Pd/Ti Schottky contact is the most common gate metallization structure. In this metallization structure, the Ti provides a stable Schottky barrier and strong bond to the GaAs, and the Au provides low electrical resistance. Au is known to diffuse at high rates into Ti, for this reason Pt, W, or Pd is used as a barrier between Au and Ti [39] .

Surface Effects:

DC life tests of unpassivated devices with Au/Pt/Ti gate structures indicate that the main failure mechanism is oxygen diffusion into the active channel area forming deep level traps [5]. In another reliability study of unpassivated power devices with Au/W/Ti gates subjected to an RF life test, catastrophic failures and a dramatic increase in reverse gate current at low reverse bias voltage were attributed to surface contamination [1]. High temperature storage tests on Si3N4 passivated devices with Au/Pt/Ti gates showed a decrease in breakdown voltage. Transconductance measurements on unstressed and stressed devices showed this to be caused by the reduction of surface states [15].

Refractory Barrier Layer:

Barrier height changes in Au/W/GaAs were shown to be larger than those of Au/Pt/Ti/GaAs when subjected to a reverse bias test [28] . DLTS and steady state I-V measurements have been reported to indicate non-reactive interface states which increase with reverse bias aging. Reactive interfaces like Ti, Pd, Al, or Cr are less prone to this aging effect.

Storage and DC life tests on devices with Au/Pt/Ti gates show the dominant failure mechanisms to be diffusion-controlled migration of the gate metal into the semiconductor (gate sinking) [25,8]. In this failure mechanism Au reaches the semiconductor by migrating around the edges of the gate fingers or by diffusing along the main grain boundaries of the barrier film. The reduction in carrier density by Au diffusion can be attributed to carrier compensation or effective channel thinning. The use of W and Pd barriers have also been report, ed to result in similar failure mechanism [2,11].

Gate Structure:

In order to reduce the gate resistance, 'I'-shaped structures are widely used. This shape is chosen to increase the cross sectional area of the gate which in turn reduces the gate resistance.

Device burnout is initiated at the drain Ohmic contact edge due to the local high current density. Thus, the burnout. voltage can be increased by adding a gate recess to thicken the active layer under the drain metal and reduce the current density at the drain metal edge. However, deeper recesses have been shown to provide less contact area between the head and stem of the gate. A theoretical structure simulation of T'-shaped gates showed a high concentration of stress in the area between the head and stem. This was confirmed in DC life tests performed on PHEMT devices with Au/Ti/Mo/Ti gates showing an increase in gate resistance and noise figure [6] .

Ohmic Contact Metallization:

Au-Ge/Ni is widely used as the Ohmic contact for GaAs based devices. The increase in source and drain parasitic resistance in devices with Au-Ge/Ni contacts has been attributed to contact deterioration[19, 10, 16, 24], Ohmic metal migration [32], and the introduction of traps [20, 21]. The data indicates that Ohmic contact degradation is not the dominant failure mechanism of mature GaAs devices.

Radiation:

Several studies have shown GaAs devices to be radiation hard [3, 4, 17]. The superlattice buffer used in HEMTs has been shown to further improve the device radiation hardness [17] . Also, it has been shown that ion-implanted material is three to five times more susceptible to the introduction of radiation-induced defects than epitaxial material [4].

SUMMARY:

A GaAs reliability database was developed. Analysis of the data indicates GaAs devices to be relatively radiation hard. The dominant failure mechanisms reported in the literature are metal-metal interdiffusion, metal -semiconductor interdiffusion, and electromigration. Table 2 shows the wide range of activation energies associated with these failure mechanisms. We intend to maintain this database current and use it as a guide for determining the reliability of devices used on future space missions.

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RFERENCES :

1- Jul-81, E.D.Cohen,A. C.Macpherson,A. Chri stou,"Rel iability of power GaAs FET's-Au Gates and Al-Au linked gates",IEEE Transaction on MTT, MTT-29,No.7, P636

2- Mar-86, C. Canali , F.Fantini, D . Ogliari, L.Umena, and E.Zanoni, 'Gate Metallization "sinking" into the active channel in Ti/W/Au Metallized Power MESFET's",IEEE Electron Device Letters, EDL-7, No.3, P185

3- Aug-80, R.J.Gutmann and J.M. Borrego, "Degradation of GaAs MESFETs in Radiation Environments", IEEE Transaction of Reliability, VOL. R-29 , NO.3 , P232

4- Dee-88, A.Meulenberg, H.A.Hung, K.E.Peterson, and W.T.Anderson ,"Total dose and transient radiation effects on GaAs MMIC's", IEEE Transaction on electron devices , Vol . 35 , No.12 , P2125

5- Oct-91, Y.Saito, G.Shimamoto, T.Trinh, and W.A.Koziarz ,"Reliability study of low-noise AlGaAs/GaAs HEMTs from three manufacturers", 1991 GaAs REL Workshop , P6

6- Oct--9l, T.Ishikawa, M.Katsumata, K.Hosogi, H.Minami, T.Kuragaki,T. Katoh, S.Orisaka, K.Nishitani, and M.Otsubo ,"Reliability study on T-shaped Gate Hemts", 1991 GaAsREl Workshop , P29

7- Oct-91, K.A.Christianson ,"Failure analysis of a life tested GaAs MMIC Amplifier", 1991 GaAs REL Workshop , P41

8- Oct.- 91, T.Hashinaga, M.Nishiguchi, and H.Nishizawa ,"Active Layer '1'binning due to Metal-GaAs Reactions in GaAs ICs with Ti/Pt/Au gate Metallization" , 1991 GaAs REL Workshop , P47

9- Apr-92, T. Sacco and S.Kayali , "HEMT devi ces for space applications" , Proceedings of the monolithic microwave integrated circuit space and ground applications symposium, P73

10- 1991, C.Canali, F.Magistrali, M.Sangalli, C.Tedesco, E.Zanoni , G.Castellaneta, and F. Marchetti,"Reliability Aspects of commercial AlGaAs/GaAs HEMTs", 1991 IEEE/IRPS, P206

11- 1986, D. Ogbonnah and A. Fraser , "Reliability investigation of 1 micron depletion mode IC MESFETs ", 1986 IEEE/IRPS, P132

12- Jan-85, J.M.Dumas, D.Lecrosnier, J.Paugam, and C.Vuchener ,"Comparative reliability study of GaAs power MESFETs: Mechanisms for surface-induced degradation and a reliable solution ", Electronics Letters , Vol.21, No.3 , P116

13- 1987, K.Hayashi, T.Sonoda, T.Yamaguchi, K.Nagahama, M.Yamanouchi, S.Takamiya, and S.Mitsui ,"Rleliability of super low noise HEMTs ", IEEE MTT-S Digest , P1023

14- Aug- 80, W.T.Anderson Jr and A.Christou , "GaAs EET failure mechanisms due to high humidity and ionic contamination ", IEEE Transaction of Reliability , Vol. R-29, N0,3 , P222

15- Apr-90, C.Canali, E.Corti, B.GabrielIi, F.Magistrali, A.Paccagnella, M.Sangalli, and C.Tedesco , "Change of gin(f) and breakdown voltage induced by thermal annealing of surface states in power MESFETs ", IEEE Transact ion on Electron Devices , Vol .37, No.4 , P1163

16- Jul-87, D. W. Lange r, A. Ezis, and A. K.Rai , "Structure and lateral diffusion of ohmic contacts in AlGaAs/GaAs high electron mobility transistor and GaAs devices ", J, Vat. Sci, Technology , B 5 (4), P1030

17- 1988, W.T.Anderson, A.Christou, F.A.Buot, J.Archer, G.Bechtel, H.Cooke, Y.C.Pao, M.Simons, and E.W,Chase , "Reliability of discrete MODFETs: Life Testing, Radiation Effects , and ESD ,1988 IEEE/IRPS, P96

18- Ott--83, T.Takeuchi ,"Reliability test report on NE673 ", NEC Corporation report , HES-33810 Rev.A

19- Apr-87, K.Togashi, H, Takakuwa, and Y.Kato , "Reliability of low noise microwave HEMTs made by MOCVD ", Microwave journal , P123

20- Apr-91, A.Christou, J.M.Hu, and W.T.Anderson , "Reliability of InGaAs HEMTs on GaAs Substrates ", 1991 IEEE/IRPS, P200

21- oct--90, W,Anderson and A.Christou , "Reliability of Advanced LAMBEFETs and HEMTs ", First european symposium on reliability of electron devices, failure physics and analysis , ESREF 90

22- May-90, M.Kihara, Manager ,"S-LEVEL QUAI(1FICA'I'1ON REPORT FOR TOSHIBA S8900B SERIES HEMTS ", Toshiba Corporation report

23- Ott- 90, R.Maurer, K.Chao, and E.Nhan , "Recent life test results on GaAs HEMTs ", 1990 GaAs Rel Workshop

24- Oct-90, W.Hu, S,Wang and T.Yu , "Reliability of 1 Ow noise AlGaAs/GaAs conventional HEMTs ", 1990GaAs REL Workshop

25- Ott- 90, J.Archer, N.Bechtel, H.Cooke and Y.Pao ,"Recent HEM]' reliability results ", 1990 **GaAs** REL **Workshop**

26- Oct-90, J.Chickanosky, E.Hilston, G.Norris, W.Coughlin, C.Barratt ,"Lifetime and failure mechanisms of a 2-6GHz MMIC amplifier ", 1990 GaAs REL Workshop

27- Oct-90, P.Ersland and D,Wells , "GaAs FET MMIC Switch reliability revisited ", 1990 GaAs REL Workshop

28- Oct-90, K,Christianson , "Contribution of surface and interface states to the *reverse* bias aging of GaAs Schottky Barriers "t 1990 GaAs REL Workshop

29- Ott-89, W.Slusark, D.McGee, R.Menna, T.Bibby, and P.Czajkowski ,"Optical screening of GaAs FETs for premature failure ", 1989 GaAs REL Workshop

30- 1989, P.Ersland and J.Parker , "The observation of gate lag in high temperature stressed GaAs MMIC switches ", 1989 GaAs REL Workshop

31- Ott-89, P.Tang, A.Milnes, and C.Bauer ,"Electromi ration in thin **films** of Au on SEMI-Insulating GaAs ", 1989 GaAs REL Workshop

32- Ott-89, T.Ishikawa, M.Katsumata, T.Fujii, Y.Mitsui, and K.Nishitani ,"A comparative study on reliability of GaAs FET with Al and Au gates ", 1989 GaAs REL Workshop

33- Ott-89, K.Chao, R.Maurer and E.Nhan , "Reliability study of gallium arsenide transistors ", 1989 GaAs REL Workshop

34- Ott-89, K.Nakahara ,"An I,-Band low-noise MMIC Amplifier using SAGFETS ", 1989 GaAs REL Workshop

35- Sep-85, A.Christou ,"Failure mechani sm study of **GaAs** MODFET devices and integrated circuits ", 1985 IEEE/IRPS , P54

36- 1988 , J.McAdoo, W.Bollen, and R.Garver , "Single--pulse RF damage of GaAs FET amplifiers ", IEEE MTT-S digest , Vol.1 , P289

37- Apr-91 , R.Maurer, C.Bargeron, R.Benson, K.Chao, E.Nhan, and D.Wickenden ,"Failure analysis of aged GaAs HEMTs ", 1991 IEEE/IRPS , P214

38- R.Murphy, W.Lindley, D.Peterson, and P.Staecker, "Performance and reliability of Ka-band GaAs lMPATT diode, P315

39- Apr-91, K.Shiojima and T.Okumura "Mapping evaluation of inhomogeneously degraded Au/PL/'l'i. ", 199'1 IEEE/IRPS , P234

40- Jun-93, H.Hasegawa, K.Katsukawa, T.Itoh, T.Noguchi and Y.Kaneko, High reliability power GaAs MESFET under RF overdrive condition, 1993 IEEE MTT-S International Microwave Symposium Digest, P.289

41- Oct-91, L.Camnitz , Improved Current Gain stability in C-doped HBTs with an AlGaAs Surface Passivation , 1991 GaAs REL Workshop

42- Aug-93, P.Dreike, D.Barton, C.Sadoval , Analysis of parametric Drift of a MESFET-Based GaAs MMIC Due to 125 C **Storage** , 1993 IEEE/IRPS ,P.345

43- Aug-93, D.Ragle, K.Decker, and M.Loy , ESD effects on GaAs MESFET Lifetime , 1993 IEEE/IRPS , P.352

44- Mar-91, W.Hu, P.Chao, M.Kao, P.Ho, R.Finke, and A.Swanson , Reliability of state-of-the-art GaAs pseudomorphic low-noise HEMTs , 1991 IEEE/ GaAs IC Symposium ,P.191

45- Aug-93, D.LaCombe, W.Hu, and F.Bardsley , Reliability of 0.1 urn INP HEMTS , **1993** IEEE/IRPS ,P.364

46- Ott--78, J.Irvin and A.Loya, Failure mechanisms and reliability of low-noise GaAs FETs, The Bell System Technical Journal, Vol.57, No.8, P.2823

47- May- 87, G.Donzelli and A.Paccagnella, Degradation Mechanism of Ti/Au and Ti/Pd/Au Gate Metallizations in GaAs MESFET's, IEEE Transaction on Electron Devices, Vol. ED-34, No. 5, P.957

48- Aug-79, I.Drukier and J.Silcox, Jr., On the reliability of power GaAs FETs, 1979 IEEE International Reliability Physics Symp.,P.150

49- Aug-79, E.Cohen and A.Macpherson, Reliability of gold metallized commercially available power GaAs FETs, 1979 IEEE Int. Reliability Physics Symp. ,P.156

50- Nov-78, A.Macpherson, K.Gleason and A.Christou, Voids in aluminum gate power GaAs FETs under microwave testing, IEEE Advanced Techniques in Failure Analysis,P.155

Table 1. Database Fields.

REFERENCE NUMBER	DC LIFE TEST TIME/RESULTS
DATE OF PUBLICATION	DC LIFE TEST TEMPERATURE
MANUFACTURER	ACTIVATION ENERGY_DCT
DEVICE TYPE	FAILURE MODE_DCT
ELECTRICAL SPECIFICATION	DC LIFE TEST FAILURE MECHANISM
TOPOLOGY	METHOD OF FAILURE ANALYSIS_DCT
GATE STRUCTURE	RF LIFE TEST (TRUE/FALSE)
TECHNOLOGY	RF LIFE TEST CONDITIONS
MATERIAL STRUCTURE	RF LIFE TEST FAILURE CRITERIA
GATE METAL	RF LIFE TEST TEMPERATURE
OHMIC METAL	RF LIFE TEST TIME/RESULTS
BACK SIDE METALLIZATION	ACTIVATION ENERGY_RFT
BONDING PAD METAL	FAILURE MODE_RFT
SURFACE PROTECTION	RF LIFE TEST FAILURE MECHANISM
MOUNTING TECHNIQUE	METHOD OF FAILURE ANALYSIS_RFT
PACKAGE	RADIATION TESTING (TRUE/FALSE)
HERMETIC (YES/NO)	RADIATION TEST TYPE
SAMPLE SIZE	RADIATION TEST CONDITIONS
STORAGE LIFE TESTST (TRUE/FALSE).	RADIATION FAILURE CRITERIA
STORAGE LIFE TEST FAILURE CRITERIA	RADIATION TEST TIME/RESULTS
STORAGE LIFE TEST TIME/RESULTS	FAILURE MODE_RT
STORAGE LIFE TEST TEMPERATURE	RADIATION TEST FAILURE MECHANISM
ACTIVATION ENERGY_ST	METHOD OF FAILURE ANALYSIS_RT
FAILURE MODE-ST	
STORAGE LIFE TEST FAILURE MECHANISM	
METHOD OF FAILURE ANALYSIS_ST	
DC LIFE TEST (TRUE/FALSE)	
DC LIFE TEST CONDITIONS	
DC LIFE TEST FAILURE CRITERIA	

Table 2. Activation Energies of Different Failure Mechanisms.

Activation Energy (eV)	Failure Mechanism	Comments	Reference Number
1.8	Migration of Ni into Al within the gate	Al/Ni gate	10
1.6	Formation of Al_3Ti within the gate	Al/Ti gate	10
1.48	Metallurgical reaction between Ti and GaAs	Al/Ti gate	18
2.0	Ohmic contact degradation (Ni/AuGe)	Formed by alloying evaporated Ni/AuGe at 450°C for 2 min.	22
0.55	Gate metal electromigration	Al/Ti gate	22
1.3	Oxygen diffusion into the active channel forming deep level traps	unpassivated device	5
1.6	Advance of the Schottky barrier into the channel	Au/Pt/Ti gate	25
1.9	Gate sinking	Au/Pt/Ti gate	8
1.05	Generation of dislocation in the strained mismatched layer	InGaAs channel of PHEMT device	20
0,85	Traps created due to exceeding the strain accommodation thickness	PHEMT	20
1	Reduction in the surface states	Si_3N_4 passivation	15
1.6	Gate metal inter diffusion into the GaAs	Au/Pd/Ti gate	11
1.79	Au diffusion into GaAs active layer through the refractory metal	Au based refractory gate	32
1.03	Ohmic metal migration	AuGe/Ni/Au Ohmic contact.	32
1.34	Sinking gate		27
1.2	Gate metal diffusion into the channel		26
1.7	Increase in source parasitic resistance	AuGeNi/Au Ohmic contact	24
0.73	Electromigration	Au strip line on [001] S.I.GaAs	31
F - X - - -	Surface contamination	Unpassivated	1
0.88	Inter diffusion of the gate metal into AlGaAs		21
1.4	Ohmic contact degradation	AuGeNi (HEMT)	21
1.5	Creation of traps in AlAs or GaAlAs layers	Laser processed HEMT	21